	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	12822	reset$4 near5 (processor or microprocessor)	USPAT; US-PGPUB	2004/02/13 16:20	
2	BRS	L2	2091	performance adj2 mode	USPAT; US-PGPUB	2004/02/13 16:20	
3	BRS	L3	1607	battery adj2 mode	USPAT; US-PGPUB	2004/02/13 16:21	
4	BRS	L4	37	2 and 3	USPAT; US-PGPUB	2004/02/13 16:21	
5	BRS	L5	4	1 and 4	USPAT; US-PGPUB	2004/02/13 16:23	
6	BRS	L6	47	1 and 2	USPAT; US-PGPUB	2004/02/13 16:23	
7	BRS	L7	34	6 and (boot$8 or initializ$5)	USPAT; US-PGPUB	2004/02/13 16:52	
8	BRS	L8	18	intel near5 speedstep	USPAT; US-PGPUB	2004/02/13 17:02	
9	BRS	L9	933	713/2.ccls.	USPAT; US-PGPUB	2004/02/13 17:02	
10	BRS	L10	1772	713/300-320.ccls.	USPAT; US-PGPUB	2004/02/13 17:03	
11	BRS	L11	1175	713/322-324.ccls.	USPAT; US-PGPUB	2004/02/13 17:03	
12	BRS	L12	318	713/601.ccls.	USPAT; US-PGPUB	2004/02/13 17:03	
13	BRS	L13	7	6 and (9 or 10 or 11 or 12)	USPAT; US-PGPUB	2004/02/13 17:07	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
14	BRS	L14	98783	power near5 (state or mode)	USPAT; US-PGPUB	2004/02/13 17:07	
15	BRS	L15	442	deep adj sleep	USPAT; US-PGPUB	2004/02/13 17:08	
16	BRS	L16	29	1 and 14 and 15	USPAT; US-PGPUB	2004/02/13 17:08	
17	BRS	L17	14	16 and (9 or 10 or 11 or 12)	USPAT; US-PGPUB	2004/02/13 17:08	
18	BRS	L18	9	17 not 13	USPAT; US-PGPUB	2004/02/13 17:09	